STX/UM96009

SAA5284 User Guide
(Version 1.0)

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USER'S MANUAL

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REVISION HISTORY

Version	Remarks
1.0	First Issue.

Purchase of Philips I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

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Preface

The SAA5284 forms a core component of data broadcasting systems that make use of the Vertical Blanking Interval (VBI).

This User's Manual describes data broadcasting in general, and the operation, programming and application of SAA5284.

The SAA5284 is a VBI and Full Field (FF) video data acquisition device tailored for application on PC add-in cards, PC mother-boards, set top boxes and as a SAA5250 replacement. SAA5284 incorporates all the data slicing, parallel interface, data filtering and control logic. It is controlled either by a parallel interface or I^2C. VBI data can be output on an ITU-R656 digital video bus.

For electrical parameters, refer to the SAA5284 data sheet.

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1 HOW TO USE THIS GUIDE TO THE SAA5284

Section 2 gives an overview of data broadcasting systems, including those that use the VBI. Following this, an overview of the SAA5284 is given with a block diagram and pin lists. To facilitate choosing how to apply SAA5284, Section 4 on Page 16 gives a flow chart that will lead to the required application circuit for a particular architecture of data broadcast receiver. A similar flow chart is contained in Section 5 on Page 17 for speedy selection of the register configurations. Finally, Section 9 on Page 29 contains a complete register map and descriptions.

Use of PC driver software for SAA5284 will be described in a separate document.

2 DATA BROADCASTING SYSTEMS

Data broadcasting is a term used for the point to mulitpoint ('one to many') broadcast of data. Today, radio and television broadcasting are the primary means of delivering information electronically to consumers.

The principal delivery mechanisms for current data broadcasting services include:

- FM broadcasting radio channels (FM subcarrier services).
- Television broadcast channels via the Vertical Blanking Interval (VBI), sideband or full field (FF).
- Cable television broadcast channels via the Vertical Blanking Interval (VBI), sideband or full channel.
- Satellite broadcast channels via the Vertical Blanking Interval (VBI), sideband or full channel (C-band, VSAT and Ku-band services).
- Telephone networks (fixed or mobile).
- Paging channels.

Data broadcasting can use all of a dedicated channel, a portion of an existing radio or television channel, or a portion of a digital channel.

Figure 1 on Page 10 illustrates the various mechanisms for supporting data broadcasting.

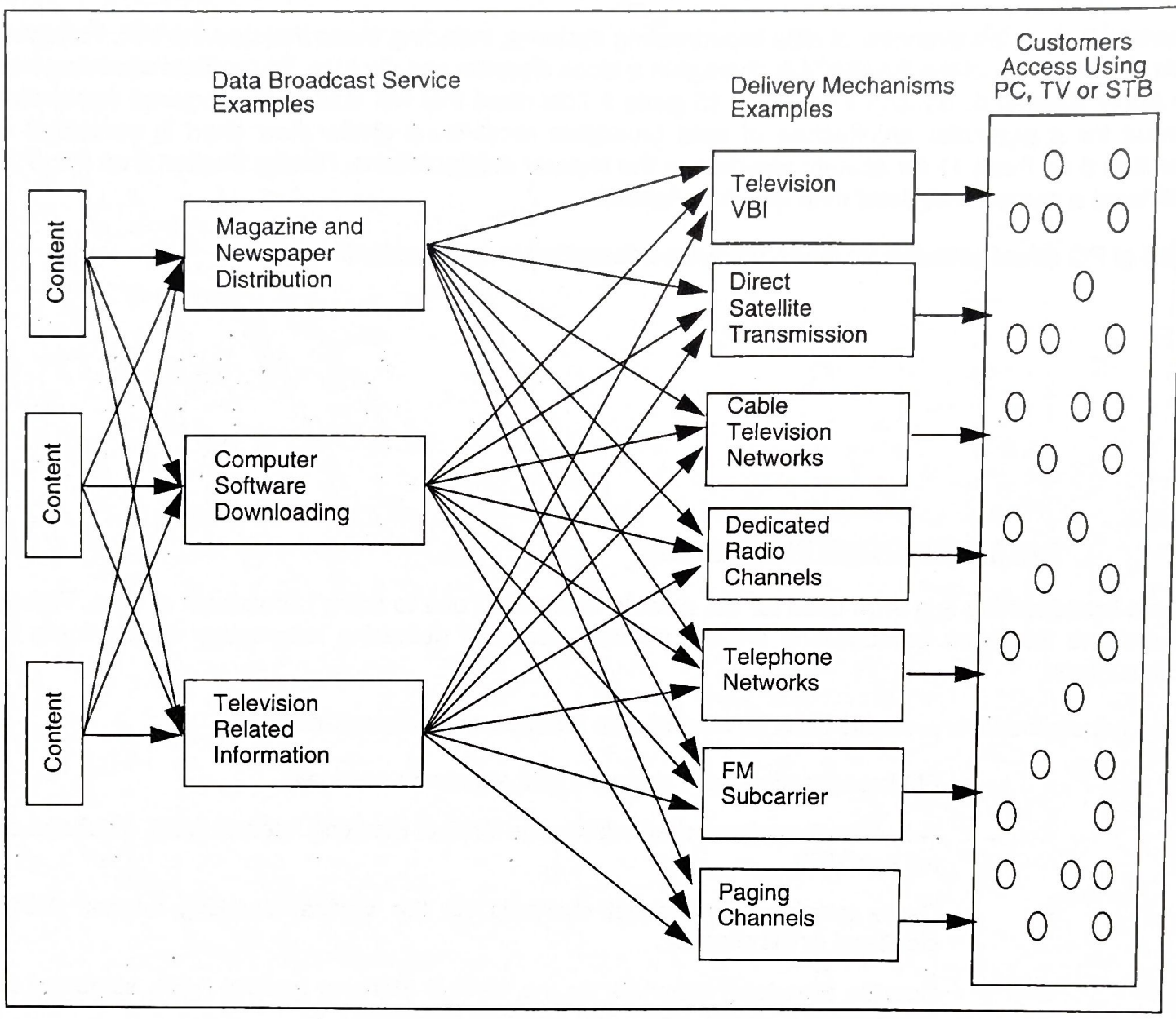

Figure 1 Data Broadcasting Delivery Mechanisms

There are a wide choice of platforms for user access systems. Some common examples are:

- Multimedia PCs.
- Dedicated TV receivers.
- Set Top Boxes.

Figure 2 on Page 11 shows a block diagram of a databroadcast system using the TV signal VBI or FF to carry data and a Multimedia PC based User Access System.

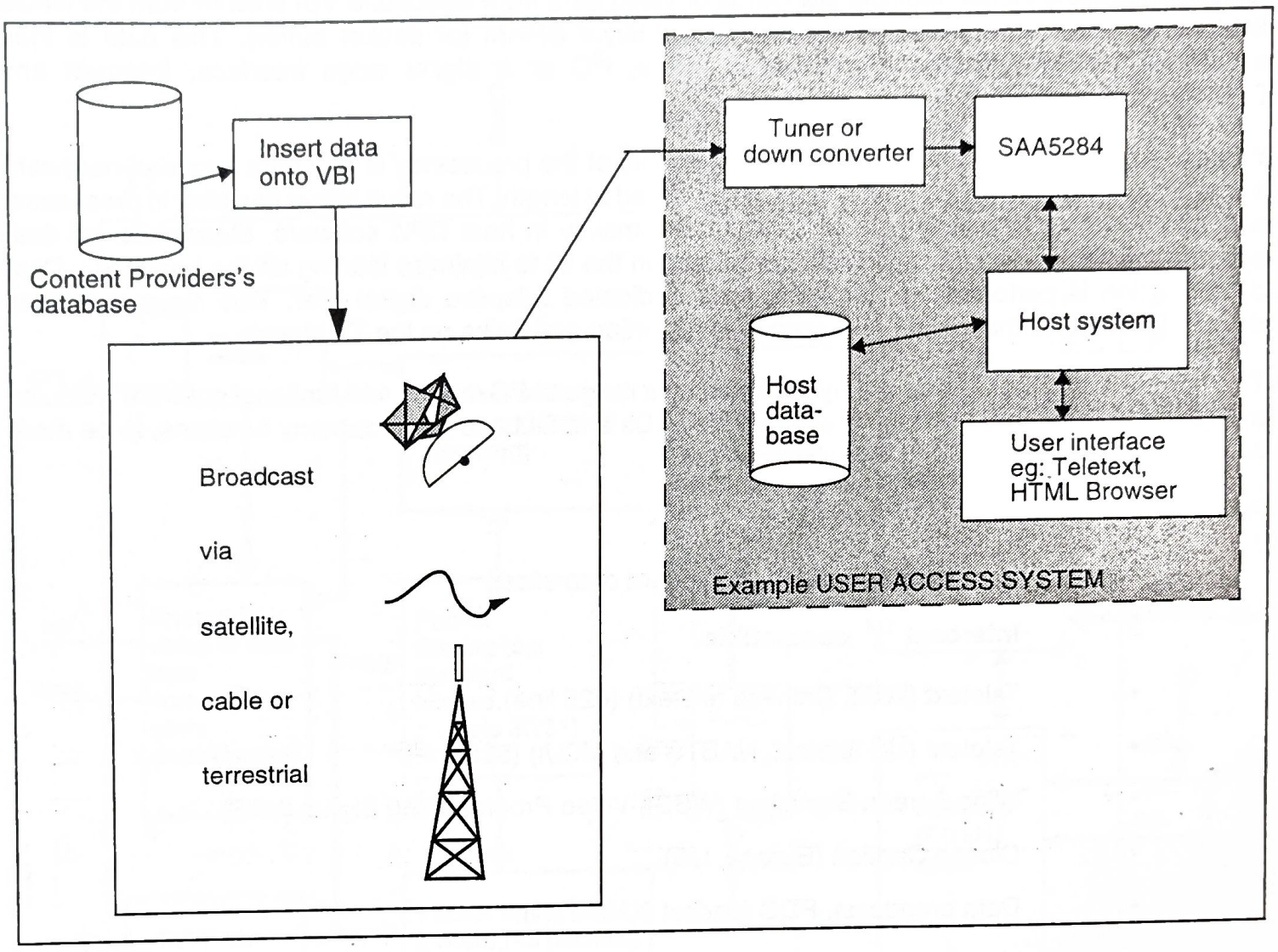

Figure 2 Typical Data Broadcast System

The PC together with the ISA add-in card provided for evaluation of the SAA5284 form a point of reference USER ACCESS SYSTEM (UAS) design, as shown in the shaded USER ACCESS SYSTEM portion of Figure 2.

The VBI data would be demodulated and stored in the SAA5284's on-board 2 kbyte RAM (known as the packet buffer). Every 40 ms[1] the host will read this data from the packet buffer (notified by interrupt or polling). Further processing of the packets to reconstruct the original data can then be performed in software on the host CPU.

3 SAA5284 OVERVIEW, FEATURE LIST AND BLOCK DIAGRAM

SAA5284 is a mixed signal full custom IC. It takes analogue baseband video (CVBS) input on one of two

1. Depending on number of VBI lines used per field.

register selectable inputs. Multiple standards of video data from selectable VBI lines or from the whole field are acquired and stored in the on-board 2 kbyte SRAM (or packet buffer). This data is then accessible via a multistandard parallel interface, I^2C or a digital video interface. Interrupt and DMA support are provided.

When designing the SAA5284, the architectural split of the processing of VBI data between hardware and software (running on the host CPU) was analysed at length. The result is that flexibility in processing acquired VBI data is maintained, as this is done mainly in host CPU software. Meanwhile, all data acquisition and caching functions are carried out on the IC to minimise loading on the host CPU. Data demodulation is performed in hardware by a dedicated adaptive digital filter. This maximises data demodulation performance in the presence of distortion and noise on the TV signal.

This hardware/software divide is fully exploited by a range of PC drivers and funtional software modules available for use with SAA5284. These include VxDs and DLLs to perform many functions, to be more fully described in the Software User Guide.

Features:

- High performance multistandard data slicer.
- **Intercast ™ compatible.**
- Teletext (WST, Chinese teletext) (625 line).
- Teletext (US teletext, NABTS and MOJI) (525 line).
- Wide Screen Signalling (WSS), Video Programming Signal (VPS).
- Closed Caption (Europe, US).
- Data broadcast, PDC (packet 30 and 31).
- User programmable data format (programmable framing code).
- 2 kbyte data cache on-board to avoid data loss and reduce host CPU overhead.
- Filtering of packets 30 and 31 standard teletext/NABTS.
- Choice of clock frequencies, direct-in clock or crystal oscillator.
- Parallel interface, Motorola, Intel, I^2C and digital video bus interface.
- I^2C control bus.
- Data transport by digital video bus.
- Choice of programmable interrupt, DMA or polling driven.
- Data type selectable video line by video line, with VBI and full field mode.
- Single IC with few external components and small footprint QFP44 package.
- Optimised for EMC.

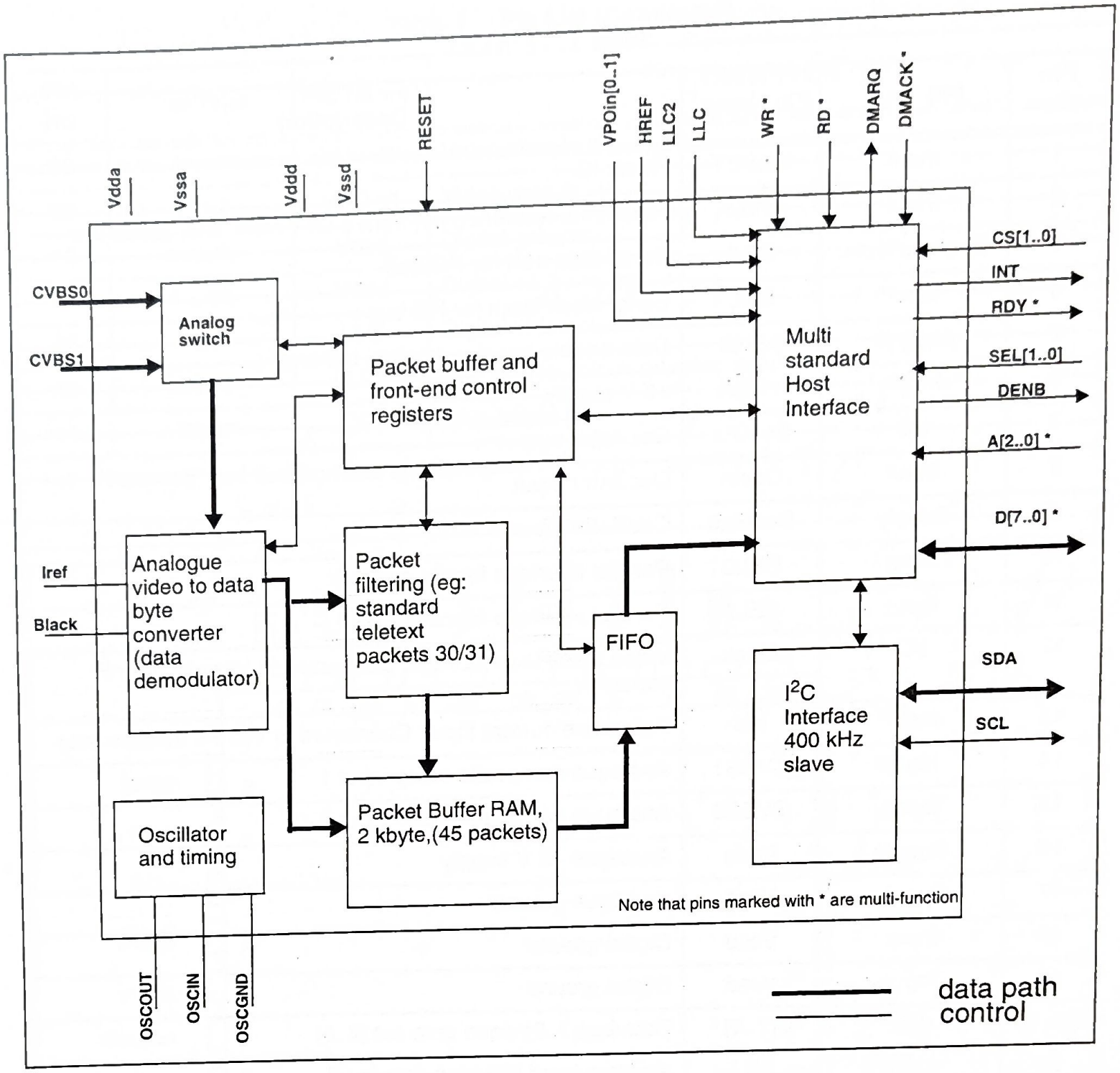

Figure 3 SAA5284 Block Diagram

Table 1 Pin List

Pin No	Pin Type	Pin Name[1]	Description
1	Input	RESET	Reset IC
2	Input	HREF	Horizontal reference pin from a DTV front-end, active low
3	Open collector	SDA	Serial data port for I^2C bus
4	Input	SCL	Serial clock input for I^2C bus
5	Output	DENB	Data enable bar (for external buffers)
6	Supply	VDDX	+5 V supply
7	I/O	OscOut	Oscillator output
8	Input	OscIn	Oscillator input
9	Supply	OscGnd	Oscillator ground
10	Input	SEL0	Parallel interface format select 0
11	Input	SEL1	Parallel interface format select 1
12	I/O	Black	Video black level storage. Connected to Vss via 100 nF capacitor
13	Input	Iref	Reference current input. Connected to Vss via 27 k resistor
14	Input	CVBS1	Analogue composite video input 1
15	Input	CVBS0	Analogue composite video input 0
16	Supply	Vdda	Analogue +5 V supply
17	Supply	Vssa	Analogue ground
18	Input	Vssd	Digital ground
19	Input	Vssd	Digital ground
20 - 27	I/O	D[7..0] *	Data bus[7..0]/video data out [7..0]
28	Input	A0 *	Address input [0]/video data in [7]
29	Input	A1 *	Address input [1]/video data in [6]
30	Input	A2 *	Address input [2]/video data in [5]
31	Output	INT	Interrupt request
32	Open collector	RDY *	Ready/DTACK (data acknowledge)/VBI
33	Input	WR *	Intel bus write/Mot bus R_W/video data in [4]
34	Input	RD *	Intel bus read/Mot bus LDS/video data in [3]
35	Input	CS0	Chip select [0]
36	Output	DMARQ	DMA request
37	Input	DMACK *	DMA acknowledge/video data in [2]

Table 1 Pin List (Continued)

Pin No	Pin Type	Pin Name[1]	Description
38	Input	VPOin0	Video data in [0]
39	Input	VPOin1	Video data in [1]
40	Supply	Vssd	Digital ground
41	Supply	Vddd	Digital +5 V supply
42	Input	LLC	Digital video clock input
43	Input	LLC2	Digital video clock qualifier input
44	Input	CS1	Chip select [1]

1. Pins with * are dual function, see description for functions separated by '/'.

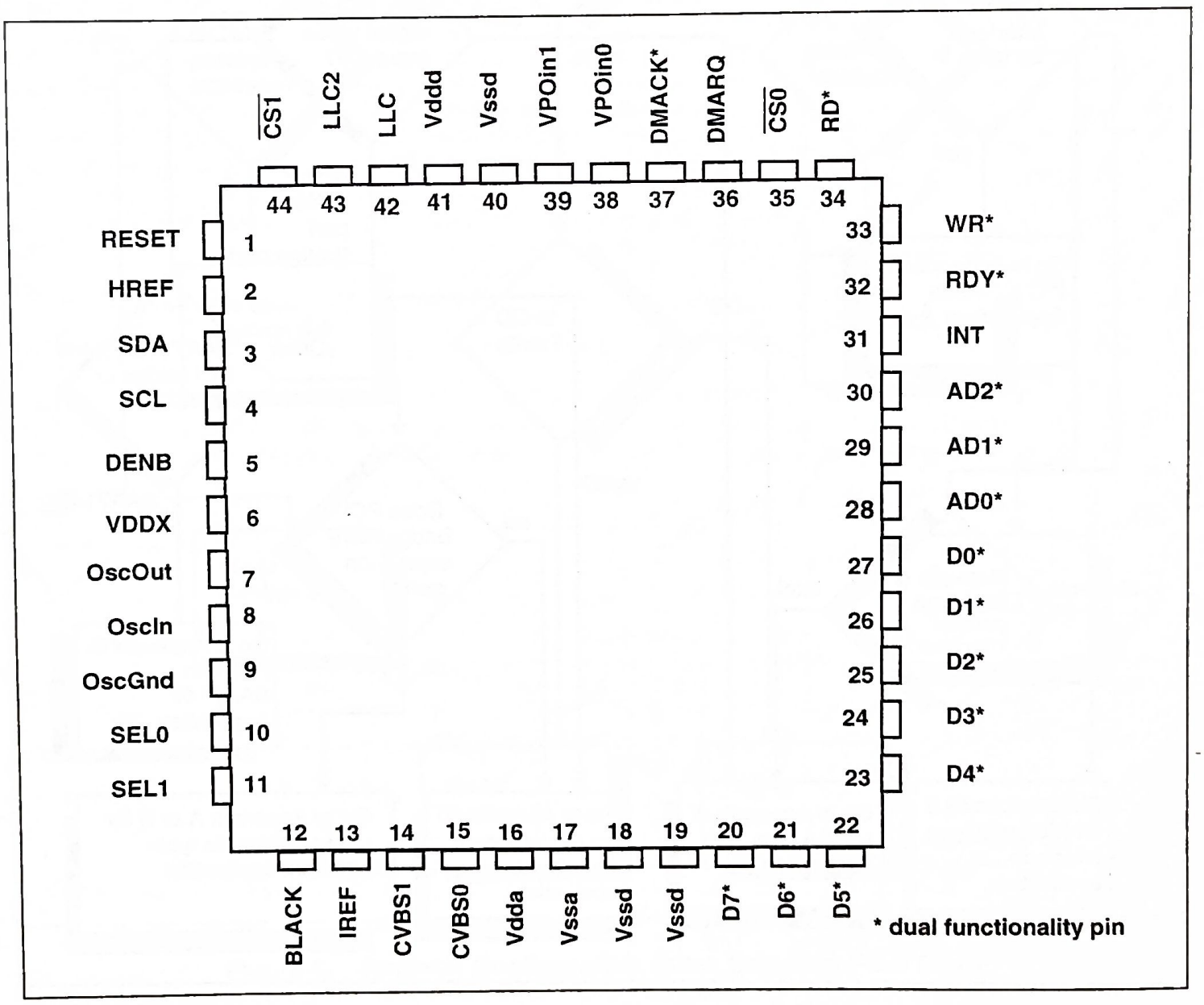

Figure 4 SAA5284 Pin Layout

4 APPLICATION CIRCUIT SELECTOR

There are many possible architectures of data broadcast receiver, from PC add-in cards to TVs to Set Top Boxes (STBs) to 8051 based. SAA5284 has numerous modes to support these architectures. This section aims to provide quick selection of the SAA5284 mode and corresponding application circuit for the required architecture. Note that the I^2C bus bandwidth is lower than that of full VBI.

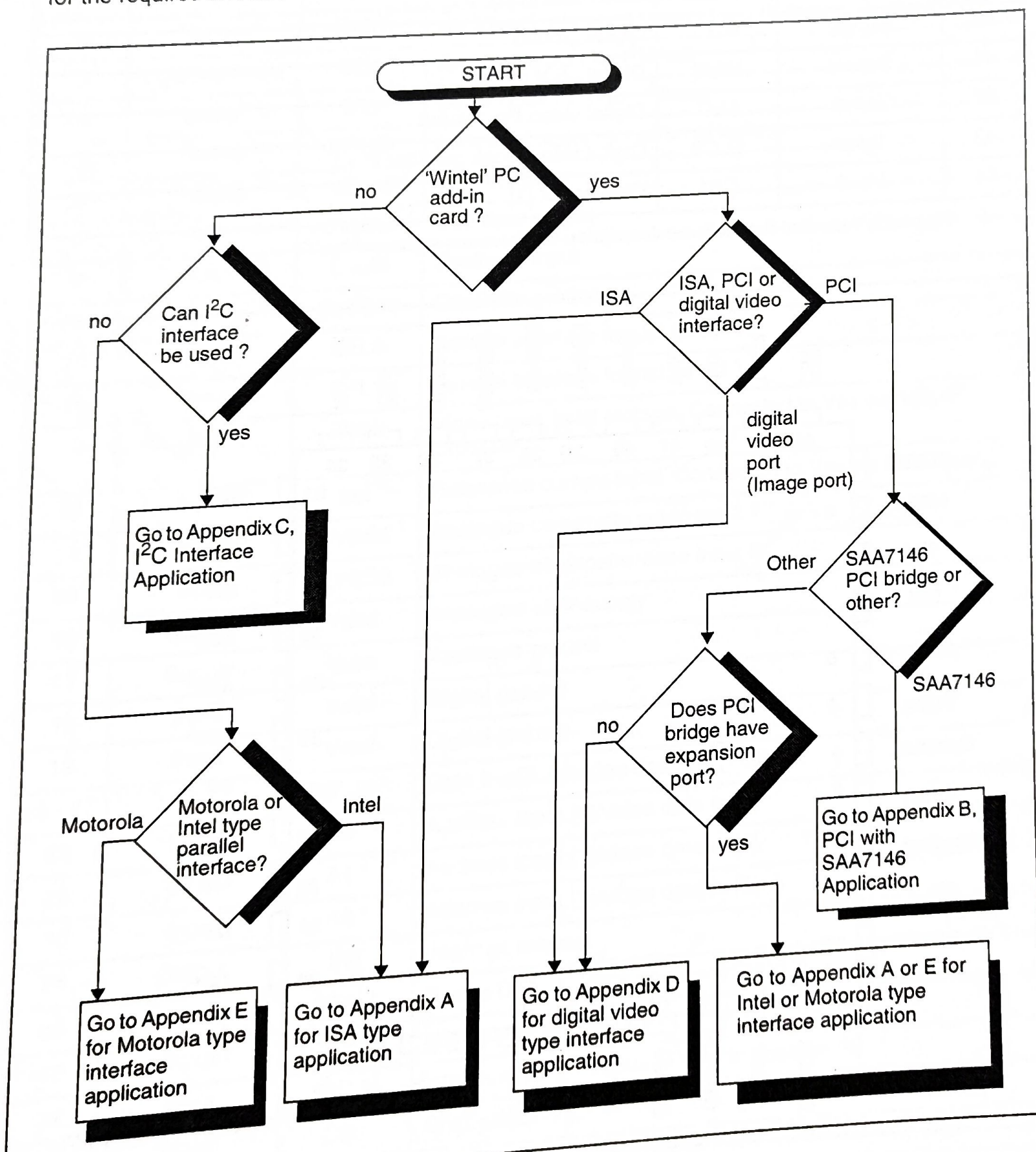

Figure 5 Application Circuit Selection Flow Chart

5 REGISTER CONFIGURATION SELECTOR

SAA5284 has 42 registers of 8 bits each. The flow chart in Figure 6 is designed to allow a fast introduction to configuring these registers for some of the most popular applications. A complete listing of register addresses and explanation of the function of each register bit is given in Section 8 on Page 24, which also describes the complete memory map of SAA5284 and structure of the VBI data when stored in the packet buffer.

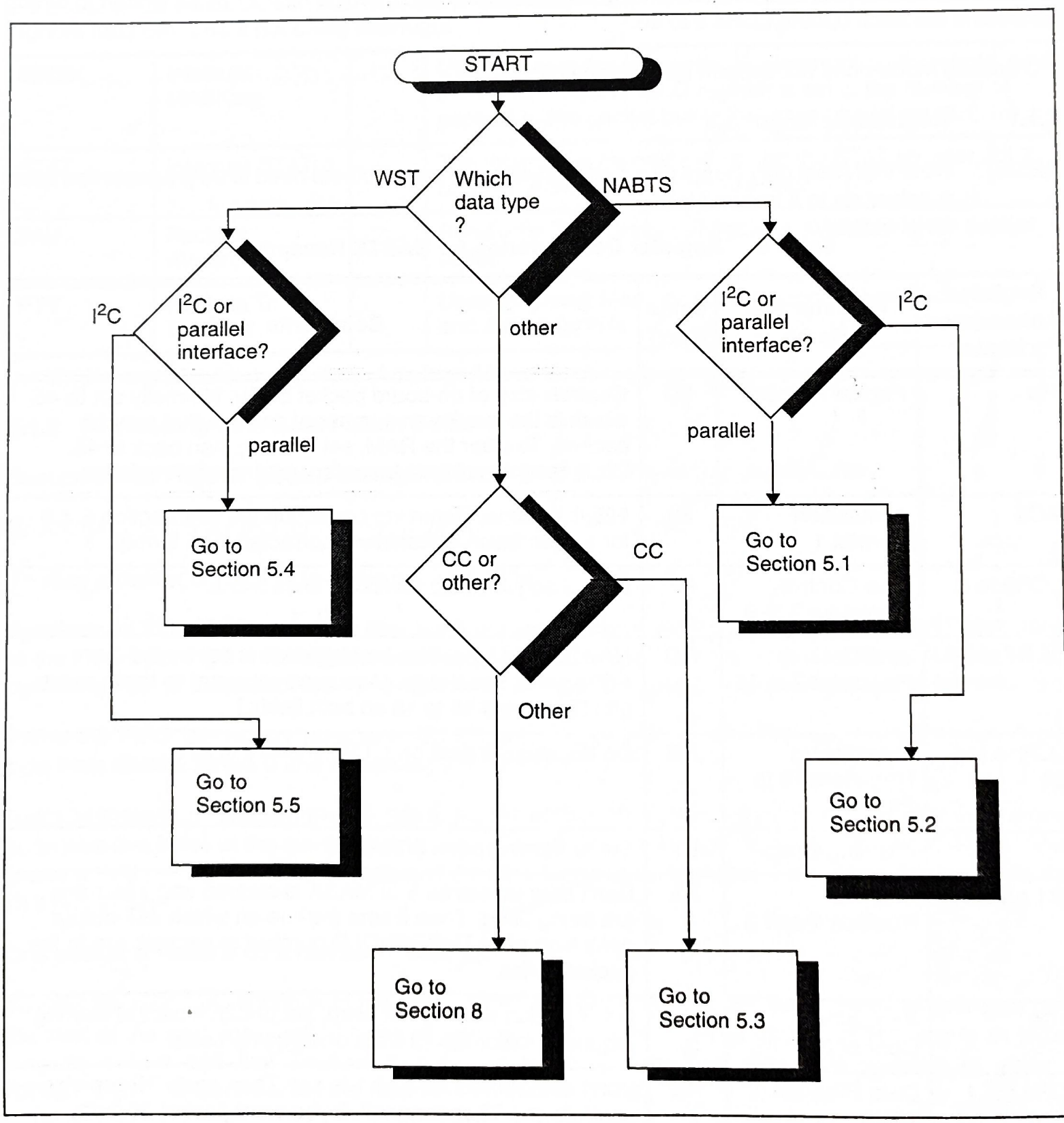

Figure 6 Register Configuration Quick Selection Flow Chart

5.1 NABTS Reception using Parallel Interface

Values to set the registers to are listed in Table 2, along with a brief explanation. Appendix H explains the different ways of accessing registers when using parallel interface mode, namely *direct addressing* and *extended addressing*.

Autoincrementing is supported in parallel access mode with all extended addresses except FFh, eg: If you wish to write to LCR2 to LCR23, write 2 to direct address 1, then the next 21 bytes written to direct address 0 will each update LCRs 2 to 23.

I^2C access mode does not support autoincrementing.

5.1.1 Register Settings

RESET: Note that reset only clears direct addressed registers, all others need to be programmed after a power on to a known state.

Table 2 Register Configuration for NABTS Reception

Register[1] Abbreviated Name	Register Full Name	Value (hex)	Comments
PN	Packet Number	2D	Controls size of on-board packet buffer. Normally set to 45, which is the maximum number of packets that may be cached. To clear the RAM, set PN = 0, then back to 45. PN is read on a frame boundary as are most registers.
AC1	Acquisition Control 1	80	525 line mode, Hamming correction off, see Section 5.4.3 for a description of hamming corrected data format.
LCR2 to 6	Line Control Registers 2 to 6	FF	Do not acquire data on NTSC lines 5 to 9.
LCR7 to 15	Line Control Registers 7 to 15	CC	NABTS data type. The framing code is set by the FC register, see below. [Assumes you want to receive data on NTSC lines 10 to 18 on both fields.]
LCR16 to 24	Line Control Registers 16 to 24	FF	Do not acquire data on NTSC lines 19 to 27.
FC	Framing Code	E7	Set to framing code of NABTS.
IP1 and IP2	Interrupt Position 1 and 2	XX	Don't care unless bit 5 of MASK is cleared and interrupts are being used. Then it sets the line on which INT output goes high after THRESHOLD number of packets are in the packet buffer.
AC2	Acquisition Control 2	00 or 02	00h if packet filtering not used, set to 02h if packet filtering required. Assumes 12 MHz clock being used.
DB1 to DB4	Data Broadcast 1 to 4	XX	Don't care unless AC2 bit 1 is set. Then each DB register controls one 'filter channel'. If you want packet 30 from magazine 1, then set to 3Eh, ie: M2, M1, M0 = 001b = magazine 1 , set R4 to R0 = 11101b = row 30.
DR	Data Received		Status register, read only. ?

Table 2 Register Configuration for NABTS Reception (Continued)

Register[1] Abbreviated Name	Register Full Name	Value (hex)	Comments
LN1 and LN2	Line Number1 and 2		Read only.
Ignore next two rows if not using interrupts			
MASK	Interrupt MASKing		Used for enabling interrupts. For interrupt on threshold, set INTT_EN. THRESHOLD register is set to the number of packets in the packet buffer that cause an interrupt.
STAT	Interrupt STATus		The interrupt is cleared by reading the STAT register. Bit 7 of STAT is the INT on threshold flag.
PAV	Packets AVailable		Read only. The number of Packets AVailable in the packet buffer.
PTT	Packets To Transfer		Used for Direct Memory Access support, see Section 9.14 and Appendix H for complete description.

1. For register address, see Table 4 on Page 24.

5.1.2 Reading Data from Packet Buffer

Section 8.4 on Page 27 gives a description of the format of data in the packet buffer.

SAA5284 contains a FIFO for reading data from the packet buffer.

To read a packet of NABTS from the packet buffer:

Synchronise to start of the current line in the packet buffer by issuing a RESET_CURRENT command to the FIFO by doing a write to direct address 1 of FEh (or, if you want to skip a line, do a RESET_NEXT by writing FDh to direct address 1). Write FFh to direct address 001b to allow the FIFO to be read.

Prime the FIFO (necessary after any RESET_NEXT or RESET_CURRENT command) by reading a byte from direct address 0 and discarding it.

Read 34 bytes from direct address 0, this is the line of NABTS data including everything after the framing code plus two bytes at the start of the packet called DI (**D**ata **I**nformation) bytes. These tell which video line and field number the data is from, and the type of the data. Section 9.10 on Page 33 describes the DI bytes in detail.

One packet of NABTS data has been read.

To read the next line, continue to read from direct address 0 and discard the 10 bytes of junk data until the start of the next line. The 10 bytes of junk data are stored because each packet buffer is 44 bytes long (to hold a 625 line Teletext packet). To avoid reading junk data, it is possible to issue a RESET_NEXT to start reading the next NABTS line.

5.2 NABTS Reception using I²C Interface

The registers are set to the same values as described in Section 5.1.1. See Table 4 for a complete register address map in I²C and parallel access modes. Section 7 on Page 23 describes in some more detail how to read from the FIFO using I²C. Note that RESET_NEXT and RESET_CURRENT I²C sub-addresses are different from the extended addresses used in parallel access mode.

I²C access mode does not support autoincrementing, so to update LCRs 2 to 23, a separate write to sub-address is required to point to each LCR in turn.

The I²C address may be 20h or 22h depending on the setting of SEL0 and SEL1 pins, see Appendix G.

5.3 NABTS and Closed Caption Reception

The registers are set to the same as Section 5.1 apart from the LCR (line control register) on which the Closed Caption signal is present. Closed Caption is normally broadcast on line 21 of the video, this corresponds to LCR18 because the **LCRs use the PAL line numbering system.**

Therefore LCR18 is set to 55h (for reception of Closed Captions on both fields, 05h for reception on field 1 only or 50h for reception on field 0 only).

As described in Section 8.4 on Page 27 the two Closed Caption bytes are stored in one 44 byte long row of the packet buffer. It may be desirable to use the RESET_NEXT FIFO command to avoid the need to read out 40 bytes of junk data.

5.4 625 line WST Reception using Parallel Interface

The values to set the registers to are listed in Table 3, along with a brief explanation. Appendix H explains the different ways of accessing registers when using parallel interface mode, namely *direct addressing* and *extended addressing*.

Autoincrementing is supported in parallel access mode, eg: if you wish to write to LCR2 through to LCR23, write 2 to direct address 1, then the next 21 bytes written to direct address 0 will each update LCRs 2 to 23.

Note that I²C access mode does not support autoincrementing.

5.4.1 Register Settings

RESET: Note that reset only clears direct addressed registers, all others need to be programmed after a power on to a known state.

Table 3 Register Configuration for Normal Teletext Reception

Register[1] Abbreviated Name	Register Full Name	Value (hex)	Comments
PN	Packet Number	2D	Controls size of on-board packet buffer. Normally set to 45, which is the maximum number of packets that may be cached. To clear the SRAM, set PN= 0, then back to 45. PN is read on a frame boundary as are most registers.
AC1	Acquisition Control 1	00	(625 line mode).
LCR2 to 6	Line Control Registers 2 to 6	FF	Do not acquire data on PAL lines 2 to 6.
LCR7 to 22	Line Control Registers 7 to 23	00	Standard Teletext data type. [Assumes you want to receive data on lines 7 to 22 on both fields.]
LCR23 and 24	Line Control Registers 24 & 24	FF	Do not acquire data on PAL lines 23 and 24.
FC	Framing Code	XX	Don't care.
IP1 and IP2	Interrupt Position 1 and 2	XX	Don't care unless bit 5 of MASK is cleared and interrupts are being used. Then it sets the line on which INT output goes high after THRESHOLD number of packets are in the packet buffer.
AC2	Acquisition Control 2	00 or 02	00h if packet filtering not used, set to 02h if packet filtering required. Assumes 12 MHz clock used.
DB1 to DB4	Data Broadcast 1 to 4	XX	Don't care unless AC2 bit 1 is set. Then each DB register controls one 'filter channel'. If you want packet30 from mag1, then set to 3Eh, ie: M2, M1 M0 = 1 = mag1 and R4 to R0 = 30 = row 30.
DR	Data Ready		Status register, read only.
LN1 and LN2	Line Number1 and 2		Read only.
Ignore next two rows if not using interrupts			
MASK	Interrupt MASKing		Used for enabling interrupts. For interrupt on threshold, set INTT_EN. THRESHOLD register is set to the number of packets in the packet buffer that cause an interrupt.
STAT	Interrupt STATus		The interrupt is cleared by reading the STAT register. Bit 7 of STAT is the INT on threshold flag.
PAV	Packets AVailable		Read only. The number of Packets AVailable in the packet buffer.
PTT	Packets To Transfer		Used for Direct Memory Access support, see Section 9.14 and Appendix H for complete description.

1. For register address, see Table 4.

5.4.2 Reading Data from Packet Buffer

Reading data from the packet buffer is performed as for NABTS, as described in Section 5.1.2.

5.4.3 Hamming Corrected Data Format

For normal teletext, the Magazine and Row bytes will be hamming decoded, ie: the first byte will contain bits 0 to 7 as follows. (This is because hamming correction is compulsory for WST. To receive WST without hamming correction, set the LCRs to 88h and bit 6 of AC1 to 1.)

bit 0 = M0, bit 1 = M1, bit 2 = M2, bit 3 = R0, bit 4 = HAM_ERROR, bit 5 to 7 = don't care.

The second byte is bit 0 = R1, bit 1 = R2, bit 2 = R3, bit 3 = R4, bit 4 = HAM_ERROR, bits 5 to 7 are don't care.

Where M0 to M2 are magazine bits and R0 to R4 are row bits. HAM_ERROR is 1 if an unrecoverable double bit error has occurred in mag/row group, single bit errors are corrected.

5.5 Normal Teletext Reception using I^2C Interface

The registers are set to the same values as in Section 5.4.1. See Table 4 for a complete register address map in I^2C and parallel access modes. Section 7 on Page 23 describes in some more detail how to read from the FIFO using I^2C. Note that RESET_NEXT and RESET_CURRENT I^2C sub-addresses are different from the extended addresses used in parallel access mode.

I^2C access mode does not support autoincrementing, so to update LCRs 2 to 23, a separate write to sub-address is required to point to each LCR in turn.

The I^2C address may be 20h or 22h depending on the setting of SEL0 and SEL1 pins, see Appendix G.

6 ADDRESSING REGISTERS IN PARALLEL INTERFACE MODE: DIRECT AND EXTENDED ADDRESSING EXPLAINED

There are three different methods used to access registers using the parallel interface. Figure H1 on Page 44 shows a diagram of these addressing methods.

1) *Direct addressing* uses the A0, A1, A2 pins to address 8 addresses.

   MASK, PAV, THRESHOLD, STAT, PTT are direct addressed.

2) *Extended addressing* uses direct addresses 0 and 1 to address the rest of the registers.

   EG: to write 44h to LCR2,
   write 2 to direct address 1, then write 44h to direct address 0.

   Extended addresses are autoincrementing, so to write 55h to LCR3, follow on with a write of 55h to direct address 0 and so on.

3) *Use of the FIFO*, reading data from the packet buffer is described in detail in Section 5.1.2.

7 HOW TO ADDRESS REGISTERS IN I^2C INTERFACE MODE

The I^2C interface is a slave type with a programmable address of 20h or 22h as described in Appendix G. Registers are accessed using sub addresses, with no autoincrementing.

I^2C sub addresses for the registers are listed in Table 4.

The main areas of difference between I^2C addresses and parallel addresses are for the direct addressed registers (eg: PAV) and the RESET_NEXT and RESET_CURRENT values as shown in Table 4.

To read data out from the packet buffer FIFO, read from sub address 7Fh. Multiple FIFO reads may be made.

To do a RESET_CURRENT, write to sub address 79h, prime the FIFO, then continue as normal to read the FIFO data.

For RESET_NEXT, do the same as above but write 78h instead of 79h, remembering to prime the FIFO as described in Section 5.1.2.

8 REGISTER AND MEMORY MAPS

8.1 Register Address Map

Table 4 Register Address Listing (Addresses in Hex)

Extended Address	Direct Address	I^2C Sub-Address	Read/Write	Register/Function Accessed
00	-	00	W/R	PN
01	-	01	W/R	AC1
02 to 18	-	02 to 18	W/R	LCR2 to LCR24
19 to 1F	-	19 to 1F	W/R	reserved
20	-	20	W/R	FC
21	-	21	W/R	IP1
22	-	22	W/R	IP2
23	-	23	W/R	AC2
-	2	72	W/R	MASK
	3	73	R	PAV
-	4	74	W/R	THRESHOLD
-	5	75	R	STAT
-	6	76	W/R	PTT
28	-	28	R	DR
29	-	29	R	LN1
2A	-	2A	R	LN2
60	-	60	W/R	DB1
61	-	61	W/R	DB2
62	-	62	W/R	DB3
63	-	63	W/R	DB4
-	1	-	W/R	Extended Address
-	0[1]	7F	R	Packet buffer FIFO
-	0	-	R/W	Extended Addressed Data
FD		78	W	Reset Next
FE		79	W	Reset Current

1. When **Extended Address** set to FF.

8.2 Register Bit Listing

Table 5 Register Bit Listing

Register	*d7*	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
PN	PN7	PN6	PN5	PN4	PN3	PN2	PN1	PN0
AC1	525/$\overline{625}$	$\overline{HAM}$	FCE	$\overline{HUNT}$	(set to 0)	-	-	-
LCR2 to LCR24	DT3 f 1	DT2 f 1	DT1 f 1	DT0 f 1	DT3 f 2	DT2 f 2	DT1 f 2	DT0 f 2
FC	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
IP1	-	V8	V7	V6	V5	V4	V3	V2
IP2	V1	V0	-	-	-	-	-	-
AC2	-	-	FECLK1	FECLK0	padding	CVBS	DBonly	-
DB1	M2	M1	M0	R4	R3	R2	R1	R0
DB2	M2	M1	M0	R4	R3	R2	R1	R0
DB3	M2	M1	M0	R4	R3	R2	R1	R0
DB4	M2	M1	M0	R4	R3	R2	R1	R0
DR	FC8V	FC7V	VPSV	PPV	CCV	--	VSQ	525R
LN1	-	-	$\overline{F1}$/F2	LN8	LN7	LN6	LN5	LN4
LN2	LN3	LN2	LN1	LN0	DT3	DT2	DT1	DT0
MASK	INTT_EN	INTDD_EN	INT_IMM	INT_CLEAR	DMA_EN	DMA_DEMAND	DMA_CLEAR	-
PAV	PAV7	PAV6	PAV5	PAV4	PAV3	PAV2	PAV1	PAV0
THRESHOLD	T7	T6	T5	T4	T3	T2	T1	T0
STAT	INTT	INTDD	DMA_STAT	-	-	-	-	-
PTT	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0

8.3 Packet Buffer and Register Memory Map

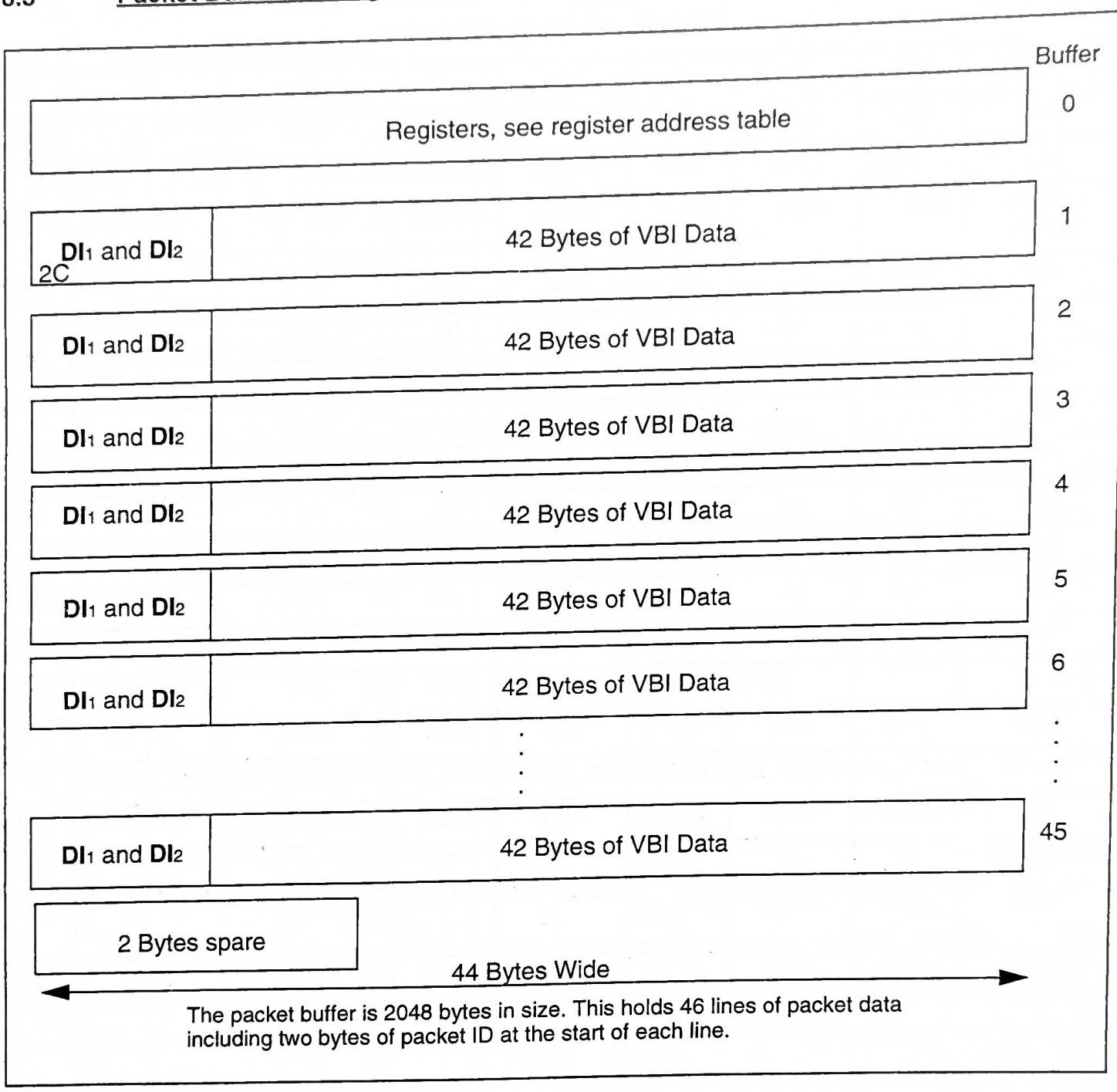

Figure 7 Packet Buffer and Control Register Map

The packet structure of the memory (ie: the format of each 44 byte segment) is described in Table 6.

8.4 Format of Data Stored in Packet Buffer

Table 6 Storage of Data in Packet Buffer

Data Type	Byte Number in Packet Buffer							
	0	1	2 3	4 15	16 27	28 35	36	37 43
Euro WST	DI1	DI2	MRAG[1] (2)	Teletext data (40)				
US WST, NABTS	DI1	DI2	MRAG[1] (2)	Teletext data (32)			Undefined (8)	
Moji	DI1	DI2	SI/PC[2] (2)	Teletext Data (33)				Undefined (7)
WSS	DI1	DI2	WSS Data[3] (14)		Undefined (28)			
VPS	DI1	DI2	VPS Data[4] (26)			Undefined (16)		
Closed Captions	DI1	DI2	CC data (2)	Undefined (40)				

1. Magazine and Row Address Group, as per WST Specification. If $\overline{\text{HAM}}$ bit = 0 (in **AC1**) (or data type is WST, see Table 11), packet buffer bytes 2 and 3 contain hamming corrected data in the lower nibble only. bit4 is set if Hamming Error.
2. SI, PC and Moji data are stored as in Table 7.
3. Wide Screen Signalling data stored as in Table 8.
4. VPS data stored as in Table 10.

Table 7 Storage of Moji Data

Byte in Packet	FC	SI	PC	Data . . .		. . .	. . . Data	
Bit Number in Packet	0 7	0 7	0 5	0 7	0 7	. . .	0 7	0 1
Bit Number in RAM		0 1 2 7	0 1 2 7	0 7	0 7	. . .	0 7	0 1 2 7
Byte No. in RAM	—	2	3	4	5	. . .	35	36

Table 8 Storage of WSS Data

WSS Bit Number	Bit 0	Bit 1	Bit 2	Bit 3	. . .	Bit 11	Bit 12	Bit 13
Bit Number in RAM	7 0	7 0	7 0	7 0	. . .	7 0	7 0	7 0
Data in RAM	xxdddddd	xxdddddd	xxdddddd	xxdddddd	. . .	xxdddddd	xxdddddd	xxdddddd
Byte No. in RAM	2	3	4	5	. . .	13	14	15

In Table 8, xx is undefined. Each dddddd are a group of 6 bits representing a single symbol (a WSS bit) bi-phase coded and then oversampled at 3 times the baud rate. To decode the individual bits, it is usual to take a majority decision on each group of 3 bits (majority of 0s or 1s), then compare the first and second three-bit groups to do bi-phase decoding. This is illustrated in the following example:

Table 9 WSS Biphase Decoding

Stored bits b5..b0	First Bit	Second Bit	Biphase Decoded	Biphase Error
111 000	1	0	1	No
000 111	0	1	0	No
101 010	1	0	1	No
101 011	1	1	—	Yes
000 011	0	1	0	No
010 000	0	0	—	Yes

Table 10 Storage of VPS Data

VPS Word and Bit Number	Word 3 *3 2 1 0 7 6 5 4*		Word 4 *3 2 1 0 7 6 5 4*		...	Word 14 *7 6 5 4*	Word 15 *3 2 1 0 7 6 5 4*	
Data in RAM	ddccbbaa	ddccbbaa	ddccbbaa	ddccbbaa	...	ddccbbaa	ddccbbaa	ddccbbaa
Bit Number in RAM	*7 0*	*7 0*	*7 0*	*7 0*	...	*7 0*	*7 0*	*7 0*
Byte No. in RAM	2	3	4	5	...	25	26	27

Each pair of bits dd, cc, bb or aa is a single symbol, biphase coded. 01 represents a 1 symbol, 10 represents a 0 symbol. 00 and 11 are biphase errors. The data can be decoded in minimum processor time by using a look-up table (256 bytes) using the received data as index, which gives the correct decoded biphase data in the ls 4 bits of each byte and 4 corresponding error flags in the ms bits; eg: a stored byte with hex value 0 x 1B (binary 00.01.10.11) would be decoded as 1001.0100 <where 1001.0100 == error_flags.decoded_bits> (ie: the middle two pairs 01 and 10 decode correctly to 1 and 0, but the outer two pairs 00 and 11 are errors).

9 REGISTER DESCRIPTIONS

Note that all unused register bits must be set to 0.

9.1 PN - Packet Number Register

(Read/Write)

d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
PN7	**PN6**	**PN5**	**PN4**	**PN3**	**PN2**	**PN1**	**PN0**

See Table 4 for address. PN defines the size of the packet buffer (in multiples of 44 byte packets). It may be written to at any time by the processor. It is acted upon on a frame boundary. Note that the minimum number is 1, in which case the start of packet write address pointer will be set to the base address = 0 + 2C (maximum 45d or 45 packets). A 0 written to **PN** effectively resets the packet buffer on the next frame boundary.

Note that it is advised to only set PN to 45d or 0. Setting PN to other values can cause PAV to increment beyond PN under certain conditions.

9.2 AC1 - Acquisition Control 1

(Read/Write)

d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
525/$\overline{625}$	**$\overline{HAM}$**	**FCE**	**$\overline{HUNT}$**	-	-	-	-

See Table 4 for address. The general control signals are written into this register at any time by the processor. The contents are read by the front-end at the start of each new frame and should be reset by software to all 0 on power on reset.

$\overline{HUNT}$ - stops amplitude searching if = 1.

FCE - select allowable errors in framing code: = 0: one error allowed, =1: no errors allowed.

$\overline{HAM}$ - disables (8, 4) hamming correction of WST mag/row group if = 1.

525/$\overline{625}$ - 525 line transmission expected if = 1.

9.3 LCR2..LCR24 - Line Control Registers

(Read/Write)

d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
DT3 f 1	**DT2 f 1**	**DT1 f 1**	**DT0 f 1**	**DT3 f 2**	**DT2 f 2**	**DT1 f 2**	**DT0 f 2**

See Table 4 for address. These registers tell the front-end what data type to receive on video lines: 2, 3, 4,... 23, (24 and after), on each field. Note that the address of the line control register in RAM is the line number.The relevant register will be read at the beginning of each line. On power on reset, the data type should be set by software to acquire nothing (DT = 1111). Registers **LCR2** to **LCR23** apply to lines 2 to 23 respectively.

Register **LCR24** applies to all lines from line 24 to the end of the field. **PAL line numbering is used,** ie: line 1 is the first line containing broad pulses at the start of field 1 (corresponding to NTSC Line 4). LCRn controls acquisition on line n+3 for NTSC line numbering.

DT3 f 1 - DT0 f 1: Data type, to be received on line n, first field.

DT3 f 2 - DT0 f 2: Data type to be received on line n, second field.

For Data Types, see Table 11.

9.3.1 Video Data Standards Supported and Corresponding LCR Setting

Table 11 Data Types

DT	Data Type	Data Rate (Mb/s)	Framing Code	FC Window	Ham Correct
0000	Teletext EuroWST, CCST	6.9375	27h	WST625	Always
0001	European Closed Caption	0.500	001b	CC625	
0010	VPS	5.00	9951h	VPS	
0011	Wide Screen Signalling bits (WSS)	5.00	1E3C1Fh	WSS	
0100	US Teletext (WST)	5.7272	27h	WST525	Always
0101	US Closed Caption (Line 21)	0.503	001b	CC525	
0110	Reserved	-	-	-	-
0111	Reserved	-	-	-	-
1000	Teletext	6.9375	prog	gen_text	Optional
1001	Reserved	-	-	-	-
1010	Reserved	-	-	-	-
1011	Reserved	-	-	-	-
1100	US NABTS	5.7272	prog	NABTS	Optional
1101	Moji (Japanese)	5.7272	prog (A7h)	Moji	
1110	Japanese Format Switch (L20/22)	5.00	prog	open	
1111	Do not acquire	-	-	-	-

9.4 FC - Framing Code

(Read/Write)

d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
FC7	**FC6**	**FC5**	**FC4**	**FC3**	**FC2**	**FC1**	**FC0**

See Table 4 for address. This register gives the framing code for the checker in the front end block. It is used if the msb of the data type DT3 is 1. It will be read at the beginning of the line after the LCR.

9.5 IP, IP2 - Interrupt Position

(Read/Write)

	d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
IP1	-	V8	V7	V6	V5	V4	V3	V2
IP2	V1	V0	-	-	-	-	-	-

See Table 4 for address. These two registers give the line number in the field of the INT signal. They are read on each frame boundary. See **MASK** register **INT_IMM** bit for turning on and off the coordination of interrupt with line number.

V8 - V0: Vertical Position of INT, Line Number (1 - 312). PAL line numbering is used.

9.6 AC2 - Acquisition Control 2

(Read/Write)

d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
-	-	**FECLK1**	**FECLK0**	**padding**	**CVBS**	**DBonly**	-

See Table 4 for address. This register controls the clock select inputs of the front end. It is read by the hardware every frame.

padding: If set to 1, padding pixels of value 42h are output until the next rising edge of the HREF input pulse, else padding pixels (value = 42h) are output onto the digital video bus until the next analogue video H-sync falling edge.

CVBS: If set to 1, CVBS1 input selected else CVBS0 input selected.

DBonly: If set to 1, only certain packets are stored, as set by registers DB1 to DB4 else all packets are stored.

FECLK1 and **FECLK0** are used to tell the adaptive digital filter that performs the data demodulation what crystal (clock) frequency is in use.

FP	FECLK1	FECLK0
12 MHz	0	0
13.5 MHz	0	1
15 MHz	1	0
16 MHz	1	1

9.7 DB1 to DB4 - DataBroadcast

(Read/Write)

	d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
DB4 to DB1	M2	M1	M0	R4	R3	R2	R1	R0

See Table 4 for address. **DB** (**D**ata**B**roadcast) registers allow control of selective acquisition of packets. For example in normal Teletext (WST) 16 channels are used comprising packets 30 and 31 of magazines 1 to 8.

M2 to 0 Magazine to acquire.

R4 to R0 Row (packet) to acquire.

Note, **DBonly** bit in **AC2** turns packet filtering on and off (it stands for **D**ata**B**roadcast **only**).

9.8 DR - Data Received

(Read)

d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
FC8V	**FC7V**	**VPSV**	**PPV**	**CCV**	**-**	**VSQ**	**525R**

See Table 4 for address. This register gives a general description of data and signal conditions within the last frame. Signals from the front-end set the relevant bits in the holding latch during the frame. On the frame boundary the contents are transferred to the data received latch and the holding latch is reset to 0. The Data Received latch may read by the processor at any time.

The bits of DR are defined as follows:

Bit	Significance if 1
525R	525-line transmission detected.
VSQ	Acquisition PLL in lock — Video Signal Quality good.
CCV	Closed Caption data received within last frame.
PPV	PALplus signalling data received within last frame.
VPSV	Video Programming Signal (VPS) data received within last frame.
FC7V	Teletext data received with 1 error in framing code within last frame.
FC8V	Teletext data received with no errors in framing code within last frame.

9.9 LN1, LN2 - Line Number

(Read)

	d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
LN1	-	-	$\overline{F1}$/F2	LN8	LN7	LN6	LN5	LN4
LN2	LN3	LN2	LN1	LN0	DT3	DT2	DT1	DT0

See Table 4 for address. These two registers contain the current line number and field. This data is written at the beginning of the new line, when the line number has settled.

$\overline{F1}$/F2, LN8..LN0 and DT3..DT0 are as defined for DI1 and DI2 below.

9.10 DI_1, DI_2 - Data Identification

(Read)

	d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
DI_1	Writing	-	$\overline{F1}$/F2	LN8	LN7	LN6	LN5	LN4
DI_2	LN3	LN2	LN1	LN0	DT3	DT2	DT1	DT0

These are the first two bytes in a packet of data read from the packet buffer FIFO (Correspond to RAM Addr: DI1 = 02Ch + n x 2Ch, and DI2 = DI1 + 1).

Table 12 Register Bit Explanation

Bits	Meaning
DT3..DT0	Type of data received (see Table 11)
LN8..LN0	Line number in current field (1..313)
$\overline{F1}$/F2	Set to "1" if field 2 of frame
Writing	Buffer in use: see note below

Writing Bit:

The **Writing** bit is set at the beginning of the line, in the same write operation as the rest of the bits of **DI1**. The **Writing** bit is reset at the beginning of the next line and written (before new values are read out of the RAM) and the register contents are written to the old start of packet address in RAM. It is commonly used by software designers to detect when the packet buffer is empty.

Wait till bit is cleared & to ensure data is ok.

9.11 PAV - Packets Available

(Read)

	d7	d6	d5	d4	d3	d2	d1	d0
PAV	PAV7	PAV6	PAV5	PAV4	PAV3	PAV2	PAV1	PAV0

See Table 4 for address. This register contains the number of packets of data available in the packet buffer FIFO. It is useful for reading before initiating a DMA transfer of packet data, or when polling the device for new data.

PAV increments as new packets are received until it reaches PN. If PN is set to a value between 0 and 45d, that is below the current value of PAV, PAV will increment beyond PN until it wraps round. Use of this functionality is not recomended.

9.12 THRESHOLD - Packets Required to Cause Interrupt

(Read/Write)

	d7	d6	d5	d4	d3	d2	d1	d0
THRESHOLD	T7	T6	T5	T4	T3	T2	T1	T0

See Table 4 for address. This register contains the number of packets that must be present in thepacket buffer to cause an INTT (**INT**errupt on **T**hreshold exceeded) interrupt.

9.13 MASK - Mask Interrupts and DMA

(Read/Write)

	d7	d6	d5	d4	d3	d2	d1	d0
MASK	INTT_EN	INTDD_EN	INTT_IMM	INT_CLEAR	DMA_EN	DMA_DEMAND	DMA_CLEAR	-

See Table 3 for address. This register contains DMA and Interrupt control and status information.

INTT_EN	Enable interrupt when number of packets in packet buffer exceeds value set in THRESHOLD register.
INTDD_EN	Enable interrupt on end of DMA read.
INTT_IMM	When 1, allows INTT interrupts to occur on any line. When 0, interrupts occur only on the line specified in **IP1**and **IP2**.
INT_CLEAR	When 1, INTT_EN or INTDD_EN self clear when an INTT or INTDD is generated respectively (ie: on the rising edge of the interrupt).
DMA_EN	Enable SAA5284 to initiate DMA. When set, reading from the packet buffer FIFO may only take place in DMA cycles.
DMA_DEMAND	When 1, demand mode else burst mode.
DMA_CLEAR	When 1, DMA_EN self clears when a DMA transfer is completed.

9.14 PTT - Packets to Transfer

(Read/Write)

	d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
PTT	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0

See Table 4 for address. This register contains the number of packets to be transferred by DMA per burst, when in DMA burst mode.

9.15 STAT - Interrupt and DMA Status

(Read)

	d7	*d6*	*d5*	*d4*	*d3*	*d2*	*d1*	*d0*
STAT	INTT	INTDD	DMA_STAT	-	-	-	-	-

See Table 4 for address. This register contains DMA and Interrupt control and status information.

INTT — Status bit to indicate that the interrupt was generated by the THRESHOLD being exceeded. Clears when STAT register is read.

INTDD — Status bit to indicate that the interrupt was generated by completion of a DMA transfer. Clears when STAT register is read.

DMA_STAT — DMA status bit. It is 1 if DMA is in progress.

10 GLOSSARY

CC	Closed Captioning
VBI	Vertical Blanking Interval
WST	World System Teletext
FF	Full Field
STB	Set Top Box
PAL	Phase Alternating Line
PDC	Program Delivery Control
WWW	World Wide Web
HTML	Hyper Text Markup Language

UAS	User Access System
Mag	Magazine

APPENDIX A

Application Circuit for ISA Card or 8051 Based System

Figure A1 shows an application circuit for a typical PC ISA add-in card type of application. Note that when using an 8051, with multiplexed address/data bus, the address is not latched in until up to a clock cycle after the transition of the RD or WR. Hence it may be necessary to control SAA5284 by port pins with appropriate modification to the 8051 based SAA5284 driver software.

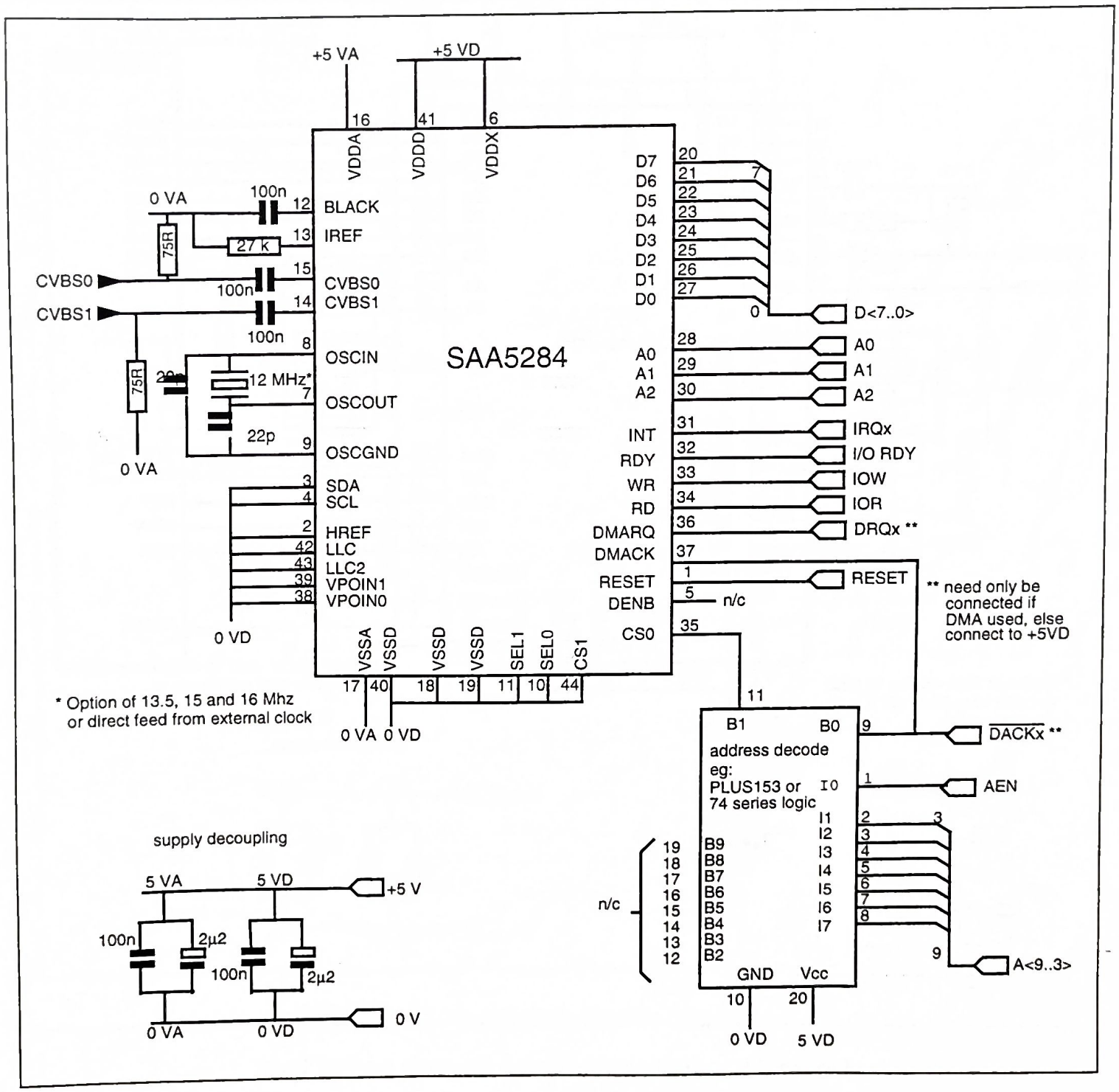

Figure A1 Application Circuit Diagram for ISA Card

Equation listing for address decode for CS0 into SAA5284:

```
B1 = / ((/I0 * I7 * I6 * /I5 * /I4 * I3 * /I2 * /I1) + /B0);
```

APPENDIX B

Application Circuit for PCI using SAA7146

This PCI application is based around the Philips SAA7146 video to PCI bridge IC. The SAA7146 has a "Data Expansion Bus Interface" (DEBI) which is an Intel/Motorola style 16-bit parallel interface. This is used to facilitate communication to SAA5284.

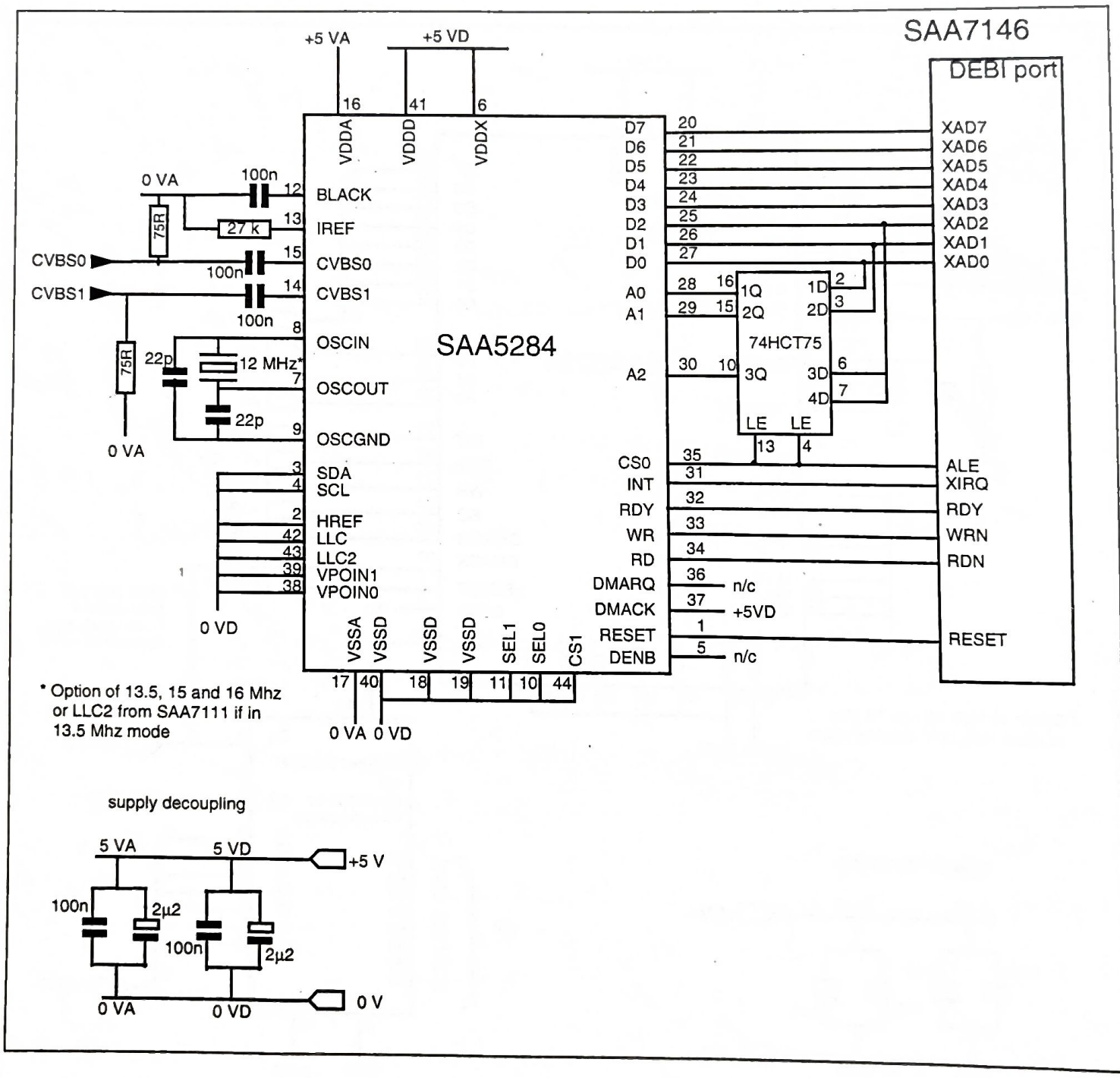

Figure B1 Application Circuit Diagram for PCI Card

APPENDIX C

Application Circuit for I²C Interface

Note that I²C address is selectable, it is 22h with SEL0 and SEL1 connected to 0 V. It is 20h with SEL0 connected to +5 V and SEL1 connected to 0 V, see Table G1.

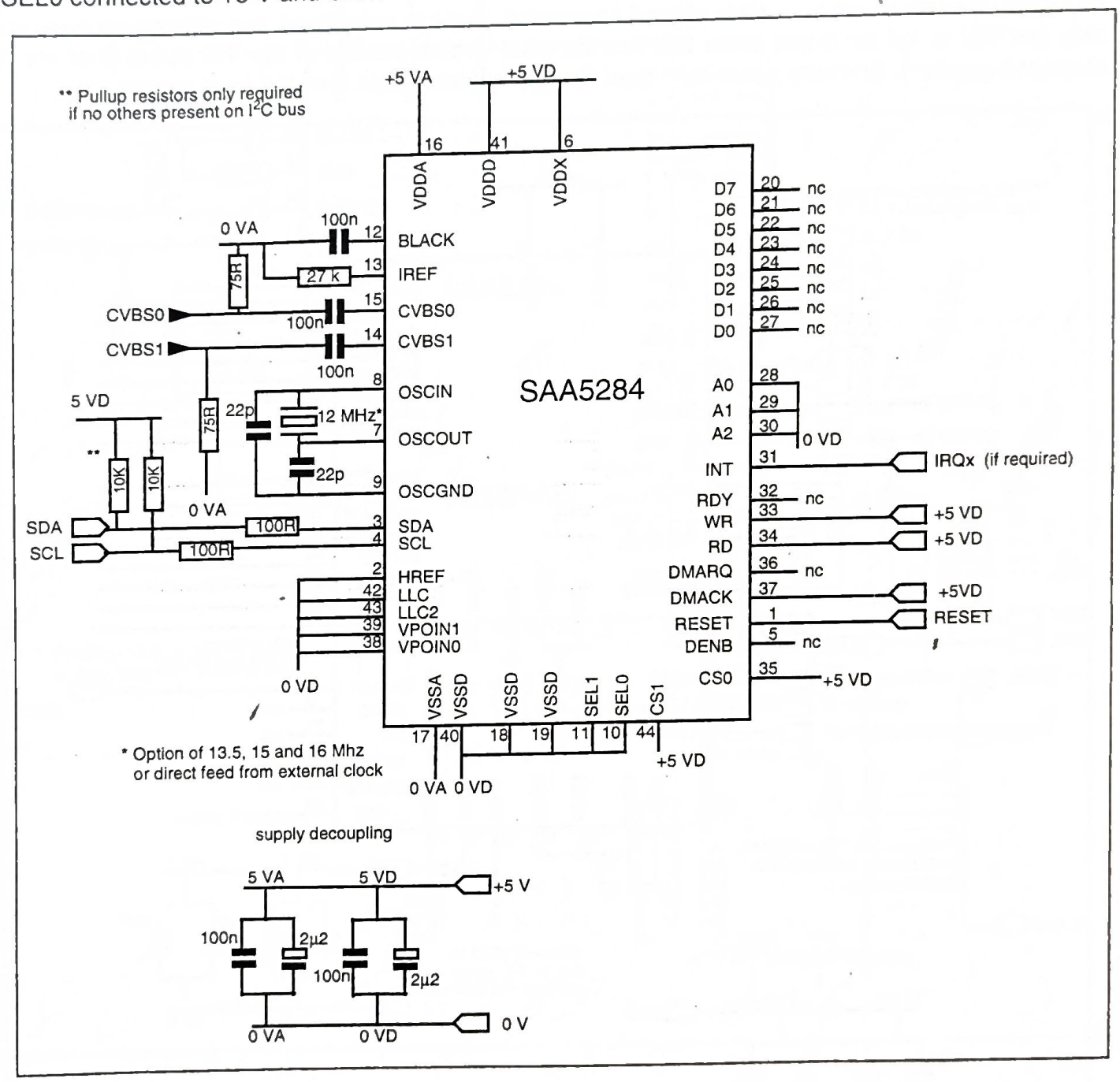

Figure C1 Application Circuit Diagram for I²C

APPENDIX D

Application Circuit for Digital Video Interface

Digital Video Mode is described in detail in Appendix J. Basically, in PCI (or other) applications where the only interface into the host system is a digital video interface, the digital video may be routed through SAA5284. SAA5284 will then pass picture information through untouched, but will demodulate video data (on VBI or full field) and place this into the pixel stream instead of the VBI pixels (that are not displayed anyway). Software would then read the demodulated data from the pixel stream.

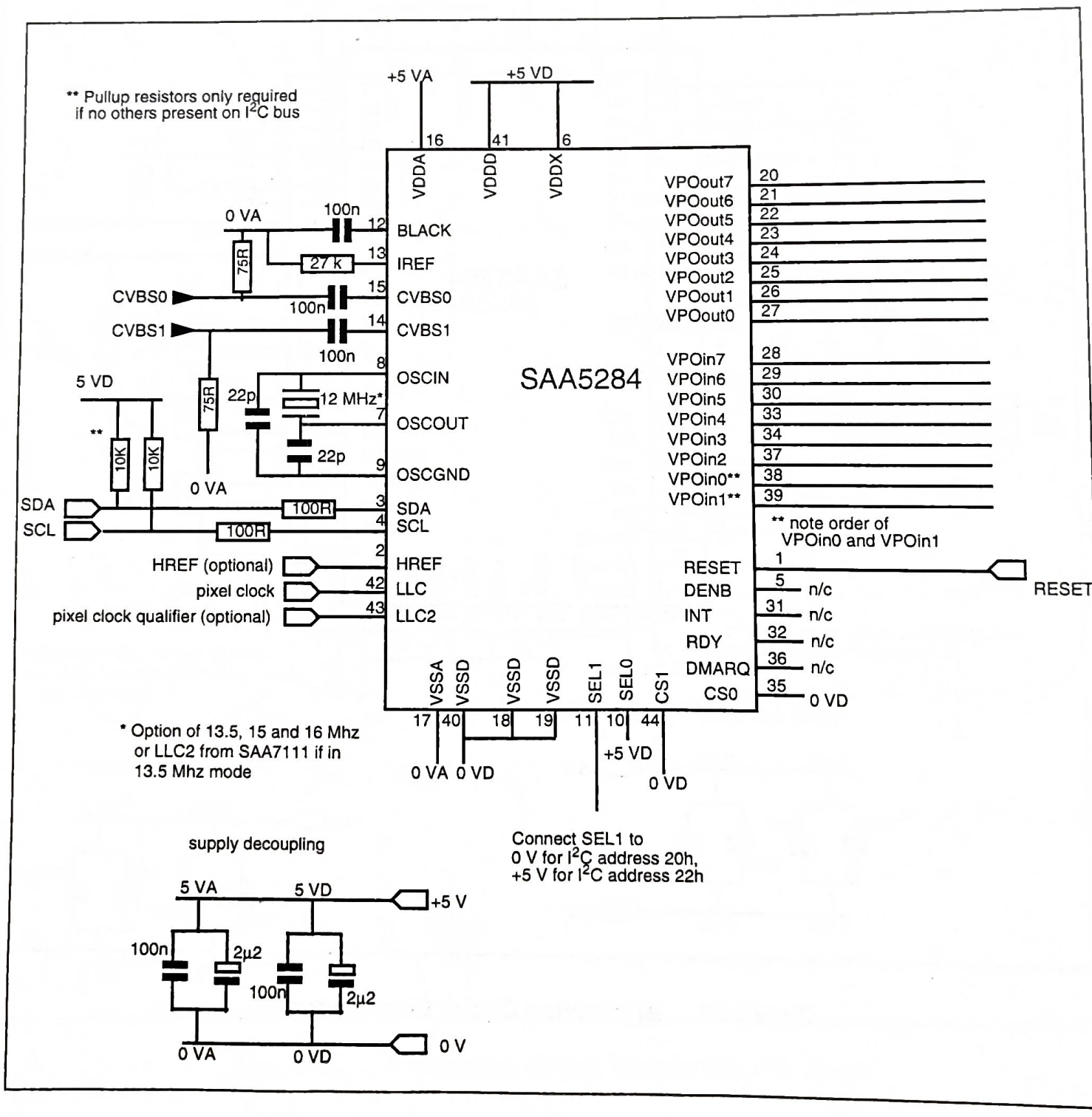

Figure D1 Application Circuit Diagram for Digital Video Interface

APPENDIX E

Application Circuit for Motorola Interface

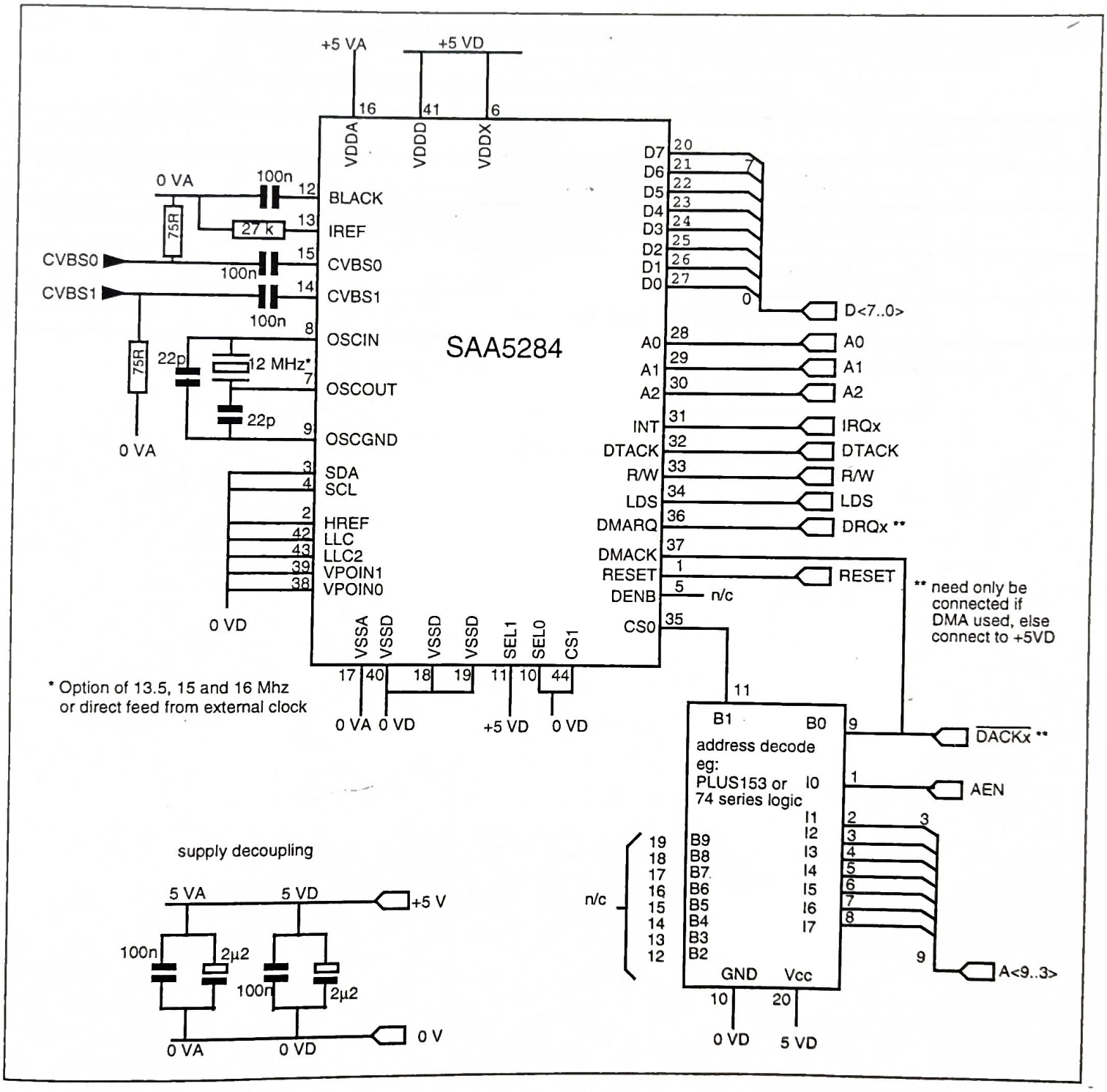

Figure E1 Application Circuit Diagram for Motorola Type Interface

APPENDIX F

Operation of SEL0 and SEL1 to Select Mode of SAA5284

Pins SEL0 and SEL1 are used to select the interface mode as shown in Table F1:

Table F1 Interface Mode Selection using SEL0 and SEL1 Inputs

SEL1	SEL0	Mode	I^2C Address
0	0	Intel type interface	0010-001X[1]
0	1	Y bus (digital video bus) interface (note different I^2C address)	0010-000X
1	0	Motorola type interface	0010-001X
1	1	Y bus (digital video bus) interface	0010-001X

1. X is read/write bit.

APPENDIX G

I²C Interface Detailed Description

400 kHz slave operation. 7-bit sub-address (msb is ignored), giving 7Fh read and 7Fh write addresses. Table 3 in the register map section lists the registers and their corresponding I²C addresses.

The I²C address is selectable using the SEL0 and SEL1 input pins, see Table G1:

Table G1 I²C Address Selection

SEL1	SEL0	I²C Address
0	0	0010-001X[1]
0	1	0010-000X
1	0	0010-001X
1	1	0010-001X

1. X is read/write bit.

APPENDIX H

Intel-Like Interface Detailed Description

Table H1 lists the pins used in Intel interface mode:

Table H1 Intel Interface Pin Description

Pin Number	Signal Name	Type	Description
20 - 27	D[7..0]	I/O	Data bus.
28 - 30	A[0..2]	I	3 address bits.
35	CS0	I	Chip select, active low.
44	CS1	I	Chip select, active low.
34	RD	I	Read, active low.
33	WR	I	Write, active low.
31	INT	O	Maskable interrupt, active high.
36	DMARQ	O	(programmable) DMA request, active high.
37	DMACK	I	DMA acknowledge input, active low.
32	RDY	Open collector	Wait to CPU, active high.
3	SDA	Open collector	I^2C data[1].
4	SCL	I	I^2C clock.

1. I^2C may be used when parallel accesses inactive.

When using Intel-like interface (and Motorola-like), two methods of addressing are used together. These are extended addressing and direct addressing. These two addressing methods are described below and in Figure H1 on Page 44.

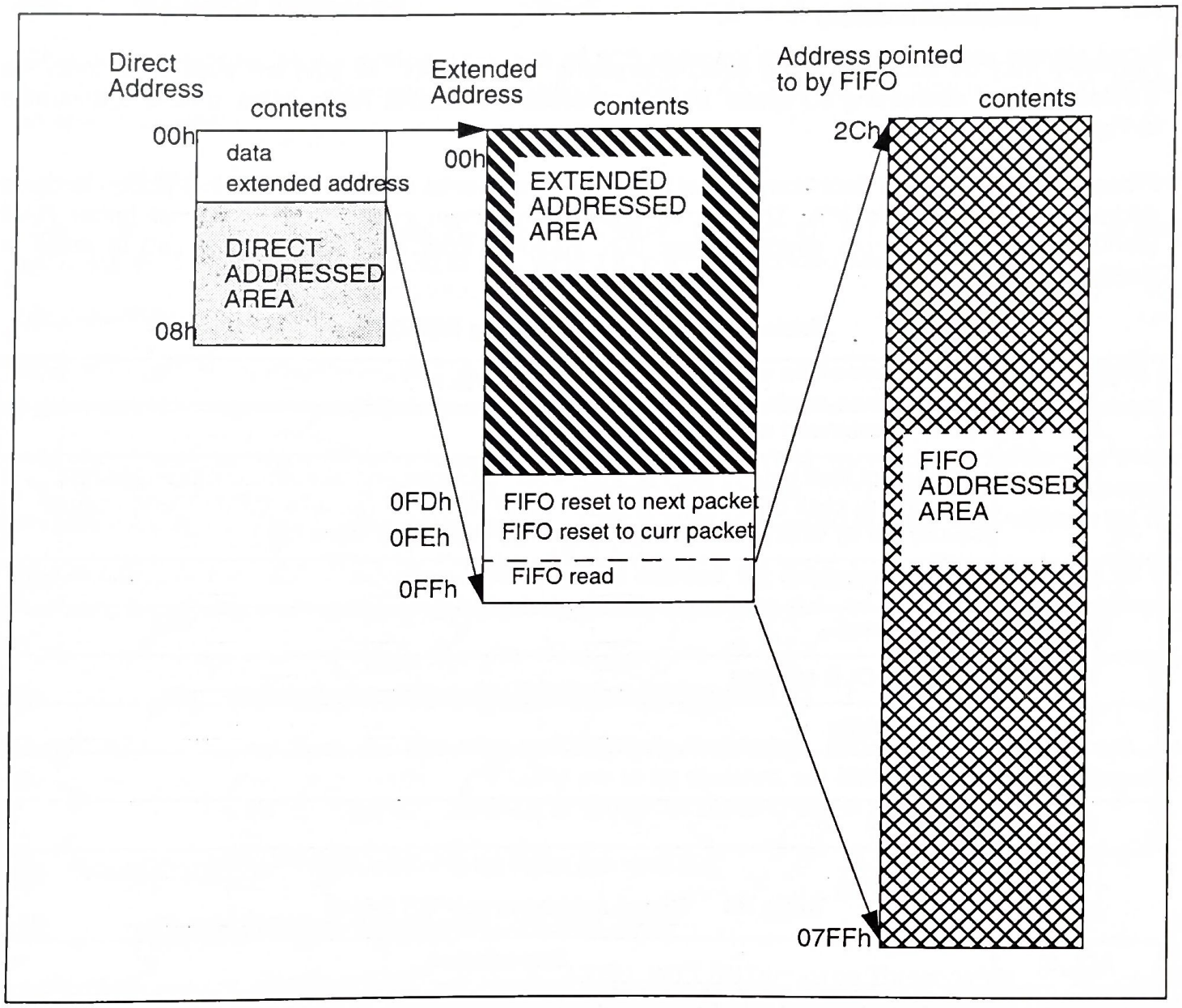

Figure H1 Memory Addressing Diagram

H.1 Direct Addressing

Registers may be accessed using direct addressing. The A0, A1, A2 pins are used to address the 8 bytes of direct addressing I/O space. Direct addresses are listed in Tables H2 and H3 and illustrated in Figure H1.

Please note that to read data from packet buffer RAM, a special extended address is written to direct address 01h (see Table H3). This allows subsequent single cycle reads of packet buffer RAM (containing VBI data) from direct address 00h. Reading from the FIFO is described in detail in Section 5.1.2.

Table H2 Direct Addressing READ Map

A(2..0)	Description
000	8 bits of extended addressed data to be read.
001	Address of next byte to read or write when using extended addressing of registers. Can only access data in packet buffer RAM via FIFO. (Access to FIFO (and access mode) set by writing special address to this byte - see Table H3.)
010	MASK register.
011	PAV register.
100	THRESHOLD register.
101	STAT register.
110	PTT register.
111	Reserved.

Table H3 Direct Addressing WRITE Map

A[2..0]	Description
000	8 bits of extended addressed data to be written.
001	Address of next byte to read or write when using extended addressing of registers. Cannot write to packet buffer RAM. Special address causes data read out to come from packet buffer FIFO, provided DMA is disabled. Special addresses are: 0FFh - read data from FIFO when reading direct address 0. 0FEh - move FIFO read pointer to start of current line. 0FDh - move FIFO read pointer to start of next line.
010	MASK register.
011	PAV register.
100	THRESHOLD register.
101	STAT register.
110	PTT register.
111	Reserved.

H.2 Extended Addressing

Extended addressing allows random access to all 2Ch registers using only 3 address signals and the 8 data signals. A map of these registers is shown in Table 4. Accesses of this type require two cycles, as described below.

Cycle1: (Write)

Write to direct address 001b (A2..A0) the extended address you wish to write to, or read from in the next cycle, eg: if you want to modify LCR2 to 34h, write 2 to point to extended address 2.

Cycle 2: (Read or write)

Read from or write to direct address 000b the value of the data you addressed in the previous cycle. In this example, LCR2 is to be set to 34h. Therefore 34h is written to direct address 000b.

In the next cycle, we have a choice. If we want to read or write to LCR3, we read or write the new value of LCR3 from or to direct address 000b. The auto-incrementing function of the extended address pointer ensures that the next extended address up from LCR2 is read or modified ie: extended address 3.

Alternatively, we may wish to modify another extended address, eg: extended address 7 (LCR7). To do this, we have to start another two cycle access as already described, but with 7 written to direct address 001.

H.3 Auto-Incrementing when using Extended Addressing

When reading from/writing to the register map via extended addressing, the address is auto-incremented where appropriate, eg: if LCRs are to be updated, set extended addressing register to 2, then write 21 bytes to direct address 000b to update all LCRs in one burst write.

The read pointer of the FIFO increments as bytes are read out.

H.4 Interrupt Support in Intel-Like Interface Mode

Two maskable interrupts are available. INTT and INTDD. INTT (**INT**errupt on **T**hreshold) is caused when the number of VBI data packets available in the packet buffer RAM reaches the number programmed into the **THRESHOLD** register. INTDD (**INT**errupt on **D**MA **D**one) is caused by DMA transfer ending.

INTT and INTDD interrupts are enabled by the INTT_EN and INTDD_EN bits respectively in the MASK register. INTDD interrupts always occur immediately at the end of a DMA transfer. INTT interrupts can be programmed to occur immediately after THRESHOLD has been reached or on a certain video line number, by setting the INTT_IMM bit in MASK and the IP1 and IP2 registers.

When an interrupt ocurs, the corresponding flag (INTT or INTDD) in STAT is set and the INT signal becomes active. If the INT_CLEAR bit is set then the appropriate enable bit (INTT_EN or INTDD_EN) in MASK is cleared. When STAT is read the two interrupt flags are cleared and the INT output is deactivated. See Section 9.13 on Page 34 for more information on interrupt support.

H.5 DMA Support in Intel-Like Interface Mode

DMA is enabled or disabled using the DMA_EN bit in the MASK register.

When demand mode DMA is enabled by setting DMA_DEMAND in MASK, a DMA transfer is requested by asserting DMARQ when PAV reaches the value stored in THRESHOLD. The transfer will continue until PAV reaches 0. Therefore in this mode an arbitary number of packets will be transferred.

When burst mode DMA is enabled by clearing DMA_DEMAND in MASK, a DMA transfer is requested immediately and the number of packets stored in PTT will be transferred.

In either DMA transfer mode, the DMA_EN bit can be automatically cleared at the end of the transfer by setting the DMA_CLEAR bit in MASK.

When DMA is enabled, access to the packet buffer FIFO (see Tables H2 and H3) using direct addressing should not be attempted. Therefore it is necessary that **DMA_STAT** should be checked if DMA is enabled simultaneously with reads from the FIFO by direct addressing. (The practice of mixing direct address reads of the FIFO with DMA reads is not recommended.)

APPENDIX I

Motorola-Like Interface Mode

Table I1 lists the pins used in Motorola-like interface mode.:

Table I1 Interface Signals in Motorola-Like Mode

Pin Number	Signal Name	Type	Description
20 - 27	D[7..0]	I/O	Data bus.
28 - 30	A[0..2]	I	3 address bits.
35	CS0	I	Chip select, active low.
44	CS1	I	Chip select, active low.
34	LDS	I	Data strobe.
33	R/W	I	Read/write.
31	INT	O	Programmable interrupt, active low.
36	DMARQ	O	(Programmable) DMA request, active low.
37	DMACK	I	DMA acknowledge input, active low.
32	DTACK	Open collector	Data acknowledge, active low.

Direct addressing, extended addressing, DMA support, interrupt support and autoincrementing are the same as in Intel-type mode.

APPENDIX J

Digital Video Interface Mode

Table J1 describes the pins used in this mode. Appendix D contains a circuit diagram for application in this mode:

Table J1 Digital Video Bus Interface Pin Descriptions

Pin No	Signal Name	Type	Description
2	HREF	I	Horizontal synchronisation pulse in (active high).
3	SDA	Open collector	I^2C data in (for control of SAA5284 in digital video interface mode).
4	SCL	I	I^2C clock.
27 - 20	VPOout(7..0)	O	Pixel data/VBI data out.
28	VPOin7	I	Pixel data in 7.
29	VPOin6	I	Pixel data in 6.
30	VPOin5	I	Pixel data in 5.
32	VBI	O	High when VBI data acquisition enabled on present line. Duration affected by **padding** bit in **AC2** (active high).
33	VPOin4	I	Pixel data in 4.
34	VPOin3	I	Pixel data in 3.
35	CS0	I	Used for direction control of dig vid bus. Tristates VPOout(7..0) if high.
37	VPOin2	I	Pixel data in 2.
38	VPOin0	I	Pixel data in 0.
39	VPOin1	I	Pixel data in1.
42	LLC	I	Pixel clock signal.
43	LLC2	I	Pixel clock qualifier signal, active high.
44	CS1	I	Used for direction control of dig vid bus. Tristates VPOout(7..0) if high.

It is important to note that the register map may only be accessed by I^2C in digital video bus mode.

When passed through SAA5284, digital video data is always delayed by one LLC cycle. This is due to resynchronisation. When using with an SAA7111 with 16-bit YUV, it may be necessary to delay the chroma by a number of samples to regain Y vs UV synchronisation.

Note that the acquired VBI data is split into two nibbles (see Figure J1), which are placed onto digital video data signals VPO0 to VPO7. VPO0 is a data available flag. It is 1 when a data nibble is present, 0 when a padding pixel is present. Software must reconstruct the original data byte from the two pixels. This is to avoid a 00h value on the ITU656 bus which the specification does not allow. VPO6 is even parity for VPO[5..0] (labelled 'P'), VPO7 is `not` P. Padding pixels will either be added until next HREF,

or until next H sync detected by the on-board sync separator, depending on setting of **padding** bit in **AC2**.

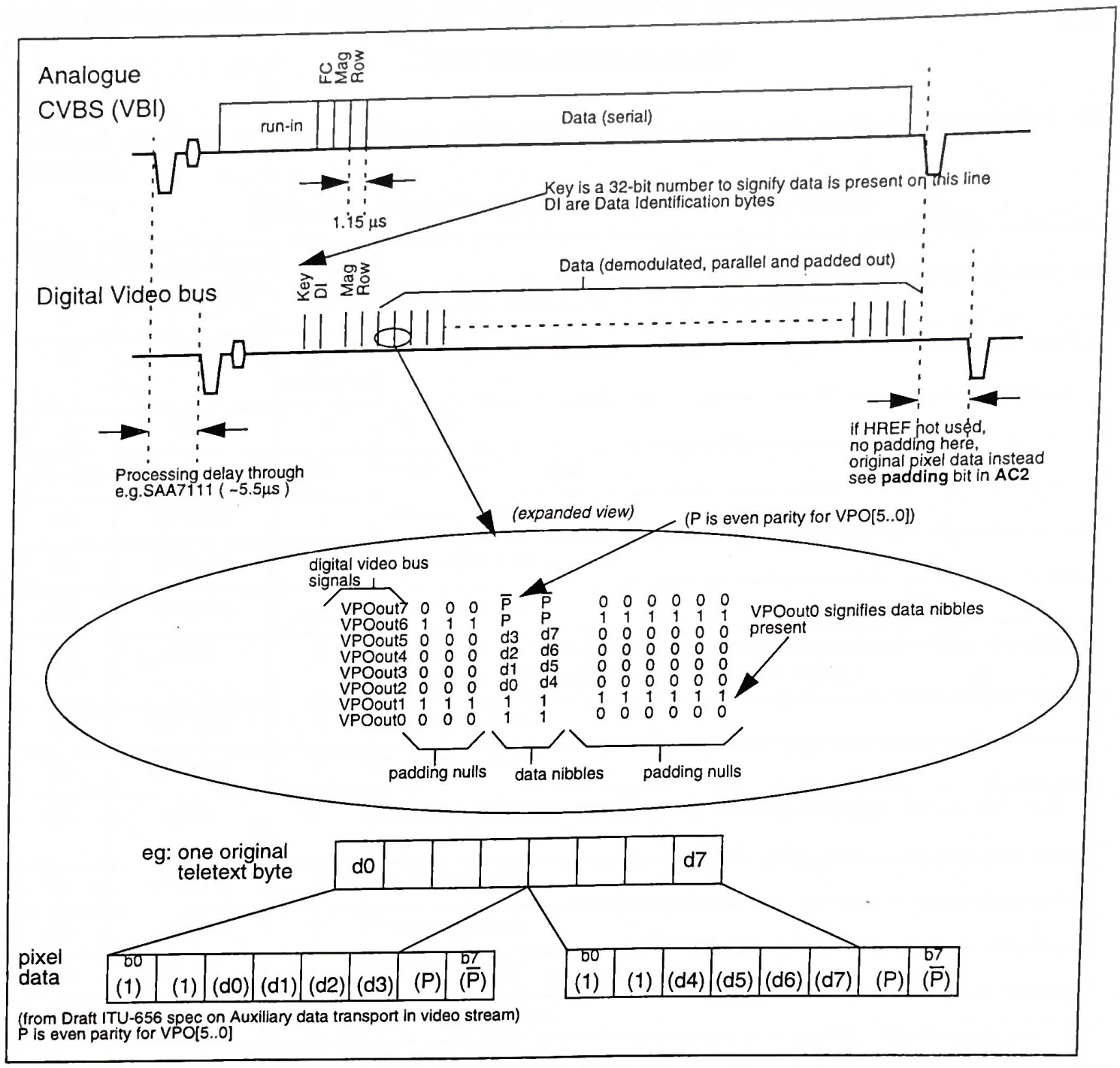

Figure J1 Description of Format of VBI Data Inserted onto Digital Video Bus

A 4 pixel key is used to signal that this line contains VBI data. The key is A5h 41h C5h 41h, in consecutive pixels. The key and (nibble-ised) DI information are placed onto the pixel bus just before the earliest possible first data byte, which is 12 µs after H sync falling edge. This means that once an H sync from the analogue CVBS is detected, 120 CLK(OSCIN clock) rising edges are counted (10 µs for 12 MHz clock or 7.5 µs for 16 MHz clock approximately), then the key bytes and DI information are placed onto the bus. DI information is also nibble-ised.

Data is only clocked in and out on rising edge of LLC with LLC2 high.

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